WHAT IS CLAIMED IS:

1. A controller for producing a sequence of states derived from an input bus, each said state comprising a plurality of independent variables realized as digital values, each said variable expressed in a corresponding digital precision and said state further characterized by duration, said controller comprising,

(a) a plurality of latched registers for receiving and retaining corresponding datums from said input bus,

(b) at least one latched mathematical register assembly for receiving and retaining corresponding datums from said input bus, said latched mathematical register assembly comprising a computational module for combining said datums in accord with a mathematical rule to yield a computed result datum, and a corresponding latched result register to retain said computed result datum, and

(c) a plurality of FIFO portions, each portion in correspondence with one said latched register and latched result register, each said latched register and result register in corresponding relationship with one said FIFO portion, whereby a FIFO assembly comprising said FIFO portions contains a sequence of said states.

2. The controller of claim 1, wherein said FIFO assembly comprises an output register and wherein a duration interval is derived from each said state, each said state persisting in said output register for said duration interval.

3. The controller of claim 1, wherein said state comprises a vector field.

4. The controller of claim 3, wherein said vector is a magnetic gradient.

5. The controller of claim 1, wherein said state comprises an RF field.

6. A controller for producing a sequence of states derived from an input bus, each said state comprising a plurality of independent variables realized as digital values, each said variable expressed in a corresponding digital precision and said state further characterized by duration, said controller comprising,

(a) a plurality of latched registers for receiving and retaining corresponding datums from said input bus and wherein at least one said latched register comprises an argument portion of said datum, an increment portion of said datum and an adder for modifying

said argument through addition of said increment portion and communication of the result thereof both to a corresponding mathematical register and to replace the value held in said argument portion of said at least one latched register,

(b) at least one latched mathematical register array for receiving and retaining corresponding datums from saidcorresponding latched register, said latched mathematical register array comprising a computational module for combining said datums in accord with a mathematical rule to yield a computed result datum, and the corresponding latched mathematical register adapted to retain said computed result datum, and

(c) a plurality of FIFO portions, each portion in correspondence with one said latched register and latched mathematical register, each said latched register and latched mathematical register in corresponding relationship with one said FIFO portion, whereby a FIFO assembly comprising said FIFO portions contains a sequence of said states.

7. The controller of claim 6, wherein said FIFO assembly comprises an output register and wherein a duration interval is derived from each said state, each said state persisting in said output register for said duration interval.

8. The controller of claim 1, wherein said state comprises a vector field.

9. The controller of claim 3, wherein said vector is a magnetic gradient.

10. The controller of claim 1, wherein said state comprises an RF field.

11. A method of controlling a system instantaneously specified by a plurality of parameters, said system including a clock device for synchronous operation, comprising the steps of:

initializing said plurality of parameters for defining each said state to default values thereof,

prescribing a progression of states at subsequent adjacent discrete times, comprising assigning a duration to each state,

characterizing each state by the changes in value from the preceding state of one or more said parameters,

transfering only said changed values to a corresponding plurality of latched data registers, said latched registers corresponding to operand parameters, and also transferring content of said

latched registers to a respective computational cell and computing the resultant of said operand parameters and retaining same in a latched resultant register,

communicating the parameters retained from each said latched register and each said resultant register and corresponding duration to an asynchronous-to-synchronous buffer,

presenting said parameters and resultants to an output in synchronous relation to said clocking device, and

maintaining said output for said corresponding duration.

12. The method of controlling the system of claim 11, wherein said operand parameters transferred to said latched registers comprise, at least, values proportional to RF phase, RF amplitude, and RF frequency.

13. The method of controlling the system of claim 11, wherein said operand parameters transferred to said latched registers comprise, at least, magnetic gradient vector magnitude and magnetic gradient vector orientation.

14. An NMR apparatus for study of the content of a sample volume, comprising:

a polarizing magnet for establishing a preferred direction for nuclear spins,

a source of RF energy controllable for selected phase, amplitude and frequency,

an RF controller comprising a clock device for synchronous operation, comprising a processor device for

initializing RF operational parameters for defining each said state to default values thereof,

prescribing a progression of states at subsequent adjacent discrete times, comprising

assigning a duration to each state,

characterizing each state by the changes in value from the preceding state of one or more said parameters,

transfering only said changed values of said RF parameters to a corresponding plurality of latched data registers, said latched registers corresponding to operand parameters, and also transferring content of said latched registers to a respective computational cell and computing the resultant of said operand parameters and retaining same in a latched resultant register,

communicating the parameters retained from each said latched register and each said resultant register and corresponding duration to an asynchronous-to-synchronous buffer,

presenting said parameters and resultants to an output in synchronous relation to said clocking device, and

maintaining said output for said corresponding duration, and

causing said output to operate said source of RF energy in accord with said output.

15. The NMR apparatus of claim 14, wherein said computational cell modifies said RF phase by an addition operation and both communicates the result of said addition back to said latched register and to said computational cell.

16. The NMR apparatus of claim 14, further comprising

magnetic gradient apparatus for imposing a magnetic gradient vector field on said sample volume, and

a magnetic vector controller comprising another processor in synchronous relation with said clock for controlling said magnetic vector apparatus to establish the orientation and magnitude of said magnetic gradient vector and maintain the persistence of said vector for a selected gradient vector duration.

17. A controller for producing a sequence of states derived from an input bus, each said state comprising a plurality of independent variables realized as digital values, each said variable expressed in a corresponding digital precision and said state further characterized by duration, said controller comprising:

a plurality of latched registers for receiving and retaining corresponding datums from said input bus, said latched registers communicating with a plurality of FIFO portions said portions including a state duration , each portion in correspondence with one said latched register, each said latched register in corresponding relationship with one said FIFO portion, and state persistence logic whereby each said state is produced at an output of said FIFO for a specified duration.

18. The controller of claim 17, further comprising an incremental state generator wherein at least one said latched register comprises an argument portion of said datum, an increment portion

of said datum and an adder for modifying said argument through addition of said increment portion and communicates the result thereof both to a corresponding said mathematical register and to re-place the value held in said argument portion of said latched register.

19. The controller of claim 17, wherein selected said FIFO portions communicate with a source of RF power and control one or all of the RF phase, RF amplitude and RF frequency.

20. The controller of claim 18, wherein selected said FIFO portions communicate with a source of RF power and control one or all of the RF phase, RF amplitude and RF frequency.